11.5 A 900MHz UHF RFID Reader Transceiver IC

I. Kipnis[1], S. Chiu[2], M. Loyer[2], J. Carrigan[2], J. Rapp[3], P. Johansson[3], D. Westberg[3], J. Johansson[3]

[1]Intel, Berkeley, CA, [2]Intel, Folsom, CA
[3]Catena Wireless Electronics, Kista, Sweden

Automatic identification procedures have become indispensable in today's service, manufacturing, purchasing, and distribution. The omnipresent barcode labels that revolutionized the identification systems many years ago are becoming inadequate because of their low storage capacity, inability to be reprogrammed, and the line-of-sight requirement to read them [1]. Near-field RFID systems using inductive coupling are fully deployed, but their read range and data rate are both limited. A nascent technology using RFID tags operating in the UHF 860-to-960MHz band is presently gaining worldwide momentum, as it offers extended range and faster data rates. Existing UHF RFID readers are built out of discrete components and consequently suffer from low level of integration. This paper describes a single-chip transceiver containing all RF, mixed-signal, and digital baseband functionality for the physical layer of a UHF RFID reader.

Figure 11.5.1 shows a simplified block diagram of the transceiver architecture. The synthesizer is an integer-N PLL with a fully integrated VCO running at 4 times the LO frequency. The loop filter is external to minimize the phase noise. The time reference is an external 24MHz TCXO. The PLL and TX DACs are running directly on the 24MHz signal while the RX ADCs and the digital core are running on a 48MHz clock generated by an integrated frequency doubler.

The biggest challenge for the receiver front-end is to handle the leakage from the full power CW signal being transmitted during reception to keep the passive tags powered up. This self-jamming signal falls in the middle of the receive band. The receiver therefore employs direct conversion to ensure that the self jammer is converted to DC at the output of the mixer. Typically the receiver needs to tolerate self-jamming signals greater than 0dBm. This requires an LNA/mixer combination with high compression point and it limits the amount of front-end gain. The large DC at the mixer output is suppressed by sample-and-hold AC-coupling capacitors. The highpass cutoff frequency is made time varying by optionally disconnecting or short circuiting one side of the capacitors. Fig. 11.5.2 shows a high-level representation of the schematic of the offset correction circuit. When the tags are initialized with a long CW signal the cutoff frequency is made large by closing the "short" switch to quickly settle the AC-coupling capacitors. When the reader is transmitting modulated data, the highpass cutoff is made close to zero by opening the "open" switch. During tag reception the cutoff is low to allow the DC suppression circuit to track slow DC variations. The advantage of three AC coupling bandwidths is that the reader can preserve the signal integrity and still offer a short TX-to-RX turn-around time. Due to the limited front-end gain, the noise performance of the IF LNA impacts the receiver noise figure. The targeted input-referred noise voltage is 3.6nV/√Hz. To achieve this value down to 10kHz, bipolar devices are used to minimize 1/f noise. The gain of the IF LNA is programmable in three 6dB steps to allow for SNR optimization of the ADC output. A tunable 5th-order polyphase Chebyshev IF filter with programmable bandwidth provides coarse channel selectivity. For class-1 [2] and ISO 18000-6C [3] operation the filter is configured as a low-pass filter with zero IF, the IF mixers are latched in transparent mode. In class-0 [4] operation the filter is in a bandpass configuration [5] centered at 2.75MHz and the IF mixer is downconverting the signal an additional 3MHz. In both cases, the IF mixer also act as a second gain-control stage with four 6dB steps.

The I and Q signals are each sampled by a continuous time 3rd-order 48MS/s ΔΣ-ADC with 1b discrete-time switched-capacitor feedback to reduce sensitivity to clock jitter [6]. The decimation chain following the ADC allows the decimation factor to be set from 16 to 128. This is to keep the ratio between the signal bandwidth and filter sample rate relatively constant for efficient use of the digital filters. Figure 11.5.3 shows a block diagram of the digital RX and TX data paths. The digital channel filter, comprised of a combination of an FIR and an IIR filter, provides additional DC suppression and narrowband channel filtering. Both filters are programmable to allow the system to be optimized for different data rates and interferer scenarios. Depending on the protocol, one of three separate demodulators are used. Class 0 is demodulated by computing a 16-bin DFT and comparing the bin powers. Class-1 Ping uses a power triggered zero crossing detector. Class-1 Scroll and all modes of ISO 18000-6C use a coherent demodulator comprised primarily of phase recovery, rate estimator, timing recovery, and matched filters. The achieved sensitivity depends on the protocol, data rate, interferer optimization as well as the level and phase of the self jammer. Typical 1% PER sensitivities range from –70 to –90dBm.

The transmitter uses a high-efficiency supply modulation architecture for DSB-ASK and a traditional linear I/Q architecture for SSB-ASK and PR-ASK. The baseband encoding and pulse shaping is done with a programmable lookup table to minimize latency. The lookup methodology is implemented using a programmable microcode sequencer, thus a single command in the TX FIFO can generate intricate waveforms. In the case of SSB-ASK transmission the real baseband signal is filtered with a Hilbert filter to create a complex I/Q signal with suppressed negative frequencies. The signal is then offset in frequency with a CORDIC to center the SSB-ASK spectrum in the channel. In DSB-ASK transmission the shaped baseband signal can be predistorted with a 5th-order polynomial to compensate for nonlinearity in the polar modulation.

The digital I and Q signals are converted into the analog domain by 1b 3rd-order 24MS/s ΔΣ DACs. The reconstruction filter is a 5th-order Butterworth with a programmable and tunable bandwidth. The filtered signal is upconverted with a traditional I/Q modulator. The I/Q modulator can be bypassed in the DSB-ASK modulation. Power control is done both in the analog and the digital domain. After the mixer, the signal is applied to a 3-stage amplifier consisting of a common-collector driver stage, followed by two common-emitter stages with on-chip inter-stage matching and on-chip harmonic trap. The same PA can operate in class A for SSB-ASK and PR-ASK and class F for DSB-ASK. Figure 11.5.4 shows a simplified schematic of the PA. In Class F, it delivers +20dBm of output power. Simulated and measured SSB-ASK spectrums for Tari = 12.5μs are shown in Fig. 11.5.5 together with the spectral mask.

The described RFID reader IC has a die size of 21mm² and is realized in a 0.18μm SiGe BiCMOS process (Fig. 11.5.7). Simulations are carried out both at system and transistor levels. Measurement results of the silicon show good correlation with system and circuit simulations. Figure 11.5.6 shows a performance summary of the transceiver measurements versus simulations. The chip dissipates 1.5W when transmitting a +20dBm signal and simultaneously receiving –85dBm tag signals in the presence of a 0dBm self jammer.

References:

[1] K. Finkenzeller, RFID Handbook, John Wiley & Sons, 2003.
[2] MIT Auto-ID Center, Class 1 RFID Tag Protocol Specification, Version 1.0.1, Nov., 2002.
[3] ISO-IEC_CD 18000-6C, Version 2.1c2, July, 2005.
[4] MIT Auto-ID Center, Class 0 RFID Tag Protocol Specification, Feb., 2003.
[5] K. Martin, "Complex Signal Processing is Not Complex," *IEEE Trans. Circuits and Systems I*, vol. 51, pp. 1823-1836, Sept., 2004.
[6] R. Veldhoven, "A Triple-Mode Continuous-Time ΔΣ Modulator with Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2069-2076, Dec., 2003.

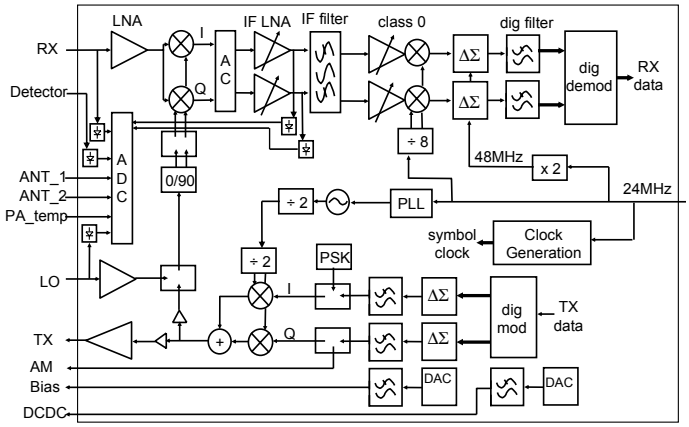

Figure 11.5.1: Functional analog block diagram.

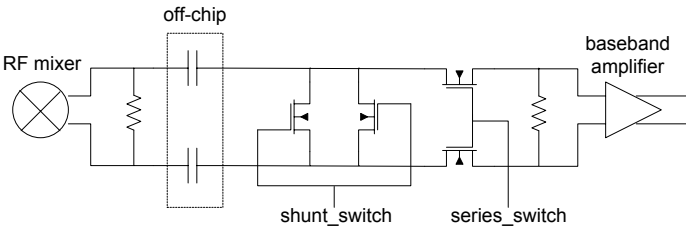

Figure 11.5.2: Simplified circuit schematic of the offset-correction circuit.

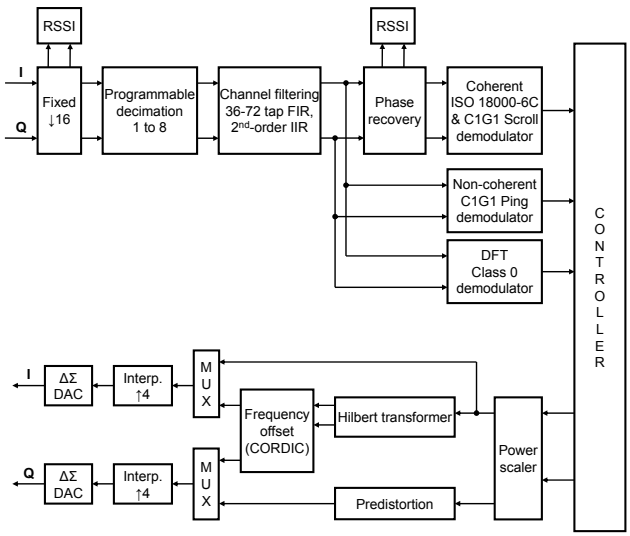

Figure 11.5.3: Functional digital block diagram.

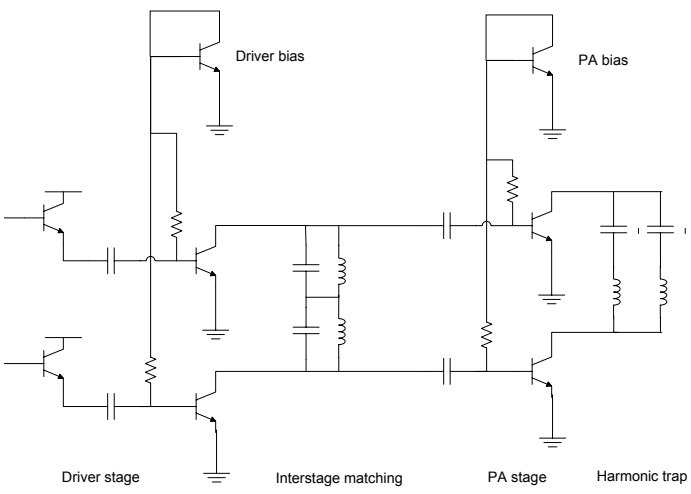

Figure 11.5.4: Conceptual circuit diagram of the PA.

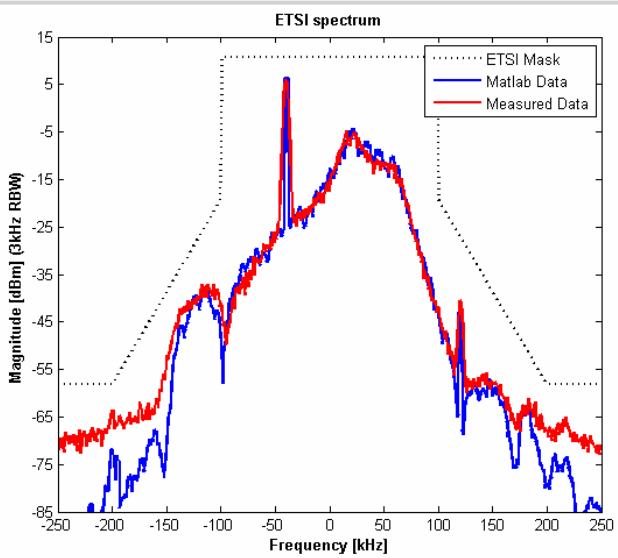

Figure 11.5.5: Simulated and measured SSB-ASK spectrum with Tari = 12.5µs.

Parameter		Simulated	Measured	Unit
Transmitter	OIP3	+29	+27	dBm
	OP_{1dB}	+20	+19	dBm
Output power	Class A	+12	+11	dBm
	Class F	+22	+20	dBm
Phase noise	@ 200kHz	−119	−116	dBc/Hz
	@ 3.6MHz	−146 VCO only	−144 VCO+PLL+TX	dBc/Hz
RF LNA/Mixer input 1dB compression point				
High-gain mode		+2	+4	dBm
Low-gain mode		+12	+11	dBm
Sensitivity, 1% packet error ratio				
FM0 40kb/s,	No self-jammer	−98	−96	dBm
FM0 40kb/s,	0dBm self-jammer	−88	−83	dBm
FM0 640kb/s,	0dBm self-jammer	−79	−78	dBm
Miller M=4 62.5kb/s,	0dBm self-jammer	−85	−85	dBm
Miller M=4 160kb/s,	0dBm self-jammer	−82	−82	dBm

Figure 11.5.6: Performance summary.

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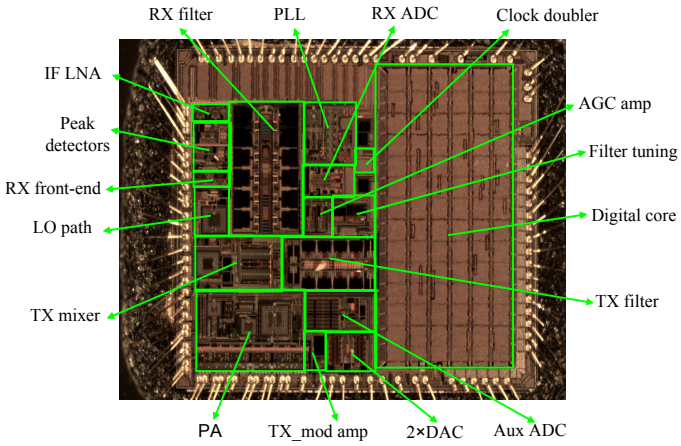

Figure 11.5.7: Die micrograph.

